5.8-GHz CMOS T/R Switches With High and Low Substrate Resistances in a 0.18-μm CMOS Process

Zhenbiao Li, Hyun Yoon, Feng-Jung Huang, and Kenneth K. O

***Abstract*—Two single-pole, double-throw transmit/receive switches were designed and fabricated with different substrate resistances using a 0.18-μm p^- substrate CMOS process. The switch with low substrate resistances exhibits 0.8-dB insertion loss and 17-dBm P_{1dB} at 5.825 GHz, whereas the switch with high substrate resistances has 1-dB insertion loss and 18-dBm P_{1dB}. These results suggest that the optimal insertion loss can be achieved with low substrate resistances and 5.8-GHz T/R switches with excellent insertion loss and reasonable power handling capability can be implemented in a 0.18-μm CMOS process.**

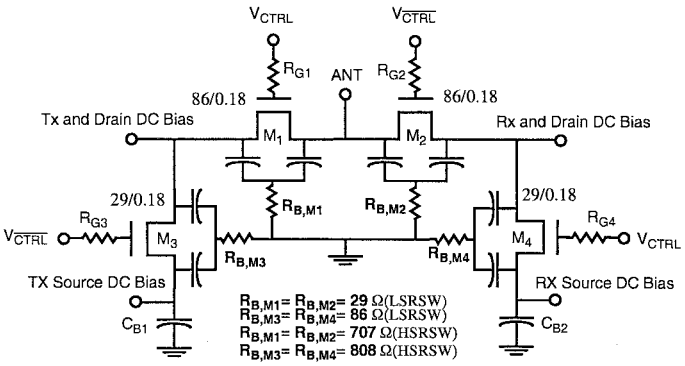
***Index Terms*—Integrated circuits, RF CMOS switch, substrate resistances, T/R switch.**

I. Introduction

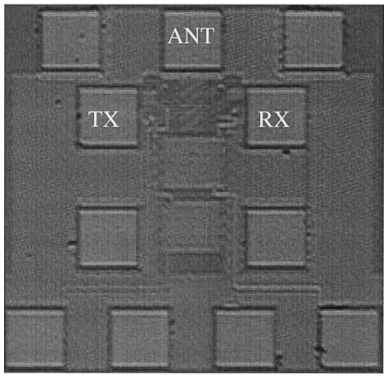
SINCE the F.C.C. allocated a 300-MHz band near 5 GHz for the Unlicensed Information Infrastructure (U-NII), the development activities of a 5-GHz CMOS receiver [1]–[3] have substantially increased. However, no progress has been made so far for the integration of CMOS switches at these frequencies, despite their key role in a transceiver.

Recent studies have shown the feasibility of implementing RFCMOS switches at 900 MHz and 2.4 GHz [4], [5]. It has been shown that the insertion loss can be minimized by either increasing or decreasing substrate resistances [4], [5]. The overall limits of substrate resistances are mainly determined by the p-well doping, substrate resistivity and layout. A low substrate resistance layout is favored on a p^+ substrate, since the maximum attainable substrate resistance is inadequate to achieve sufficiently low insertion loss, whereas sufficiently high substrate resistance may be achieved in a p^- substrate for acceptable insertion loss.

In order to examine the potentials of 0.18-μm CMOS switches near 5 GHz, as well as the effects of substrate resistance, two 0.18-μm CMOS switches were fabricated utilizing 20-Ω-cm p^- substrates with near the maximum and minimum substrate resistances that can be obtained in the process. The high substrate resistance switch (HSRSW) exhibits 1-dB insertion loss and 18-dBm P_{1dB} point at 5.825 GHz, in comparison to 0.8-dB insertion loss and 17-dBm P_{1dB} point displayed by the low substrate resistance switch (LSRSW). LSRSW is the first bulk CMOS switch to have an insertion loss less than 1 dB up to 5.825 GHz.



(a)



(b)

Fig. 1. (a) Circuit schematic of an SPDT T/R switch including key substrate resistances (R_B: substrate resistance). (b) A microphotograph of the LSRSW.

II. T/R Switch Design

Key figures of merit of a T/R switch include insertion loss, isolation and power handling capability measured by power 1-dB compression point (P_{1dB}). As shown in Fig. 1, the schematic of an SPDT RF T/R switch is similar to the previously reported 900-MHz and 2.4-GHz switches [4], [5]. In Fig. 1, the capacitors except C_{B1} and C_{B2} are parasitic capacitors of transistors and R_Bs are substrate resistances. C_{B1} and C_{B2} are by-pass capacitors to ac ground sources of M_3 and M_4. The transistor sizes are also listed in the figure.

The effects of substrate resistances on CMOS switch were explained in reference [6]. In this implementation, HSRSW utilizes only one substrate contact for each transistor to achieve as high substrate resistances as possible. On the other hand, large substrate contacts were used in LSRSW to minimize substrate resistances. Fig. 2 shows substrate contacts in LSRSW

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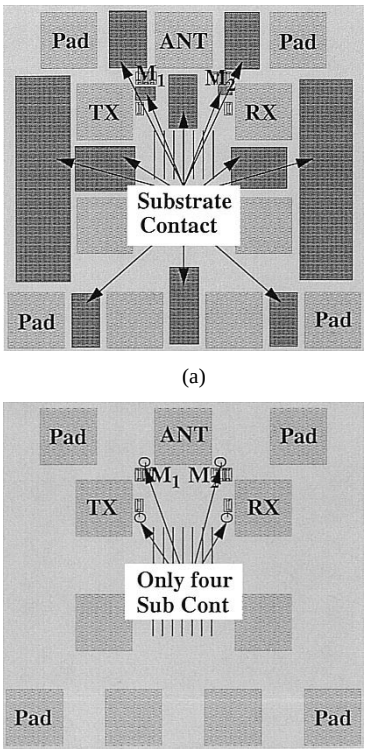

Fig. 2. Switch layouts: Pads and substrate contacts. (a) LSRSW. (b) HSRSW.

and HSRSW. The majority of the LSRSW area is occupied by substrate contacts. On the contrary, HSRSW only has four substrate contacts. Fig. 1 also includes a list of measured values of the key substrate resistances. For $R_{B,M1} = R_{B,M2}$, the measured substrate resistances are 29.3 Ω and 707 Ω for LSRSW and HSRSW, respectively. For $R_{B,M3} = R_{B,M4}$, the measured substrate resistances are 85.6 Ω and 808 Ω for LSRSW and HSRSW, respectively. The resistances are measured using test circuits identical to the switches except that the drain/source-to-body junctions are replaced with p^+ substrate contacts [7].

The substrate resistances also affect isolation. The low substrate resistances provide a low impedance path between the signal and ground leading to better isolation. The switch power handling capability (P_{1dB}) depends on dc bias of TX and RX nodes. The P_{1dB} can be limited by potentially three effects: 1) the input signal is so large that drain/source-to-body junctions of M_1/M_2 are forward biased; 2) M_3 or M_4 is unintentionally turned on and input signal has a path to ground; 3) the voltage across gate oxide is too large to guarantee its long term TDDB reliability [8]. For a given dc bias V_{DC}, conditions 2 and 3 set conflicting requirements for $V_{CTRL}/V_{\overline{CTRL}}$. Without losing generality, if Tx to antenna path is assumed to be on, i.e. V_{CTRL} is high, then the condition 2 requires $V_{\overline{CTRL}}$ small to keep M_2 and M_3 turned off all the time, but condition 3 needs $V_{\overline{CTRL}}$ sufficiently high to limit the voltage across the gate oxide. The dc bias conditions are evaluated from simulations. As V_{DC} and V_{CTRL} are set to 1.8 V and 3.6 V, respectively, $V_{\overline{CTRL}}$ is chosen as 1.3 V. Under this condition, the peak voltages across gate oxide never exceed 2.5 V, which is safe from the TDDB reliability point of view [8]. Fig. 1(b) is a micro-photograph of the

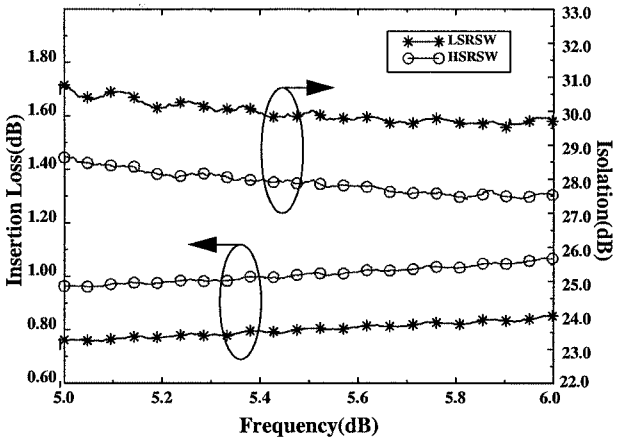

Fig. 3. Measured insertion loss and isolation for HSRSW and LSRSW.

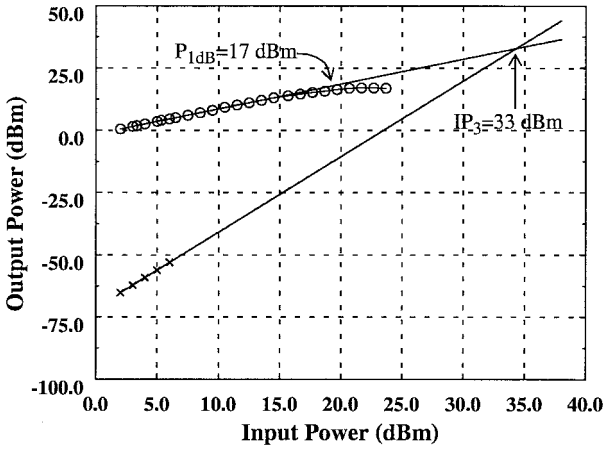

Fig. 4. Output 1-dB compression point and IP_3 measurements of LSRSW at 5.825 GHz.

LSRSW which integrates the transistors, resistors, and capacitors. The chip area is 473×451 μm^2.

III. Experimental Results

The switch measurements are performed on wafer. Fig. 3 shows the measured insertion loss and isolation. The insertion loss is about 0.8 dB for LSRSW and is 1.0 dB for HSRSW, and the isolation is more than 29 dB for LSRSW and is 27 dB for HSRSW, both at the same operating frequency of 5.825 GHz, and at V_{CTRL} or $V_{GB} = 3.6$ V and drain/source-to-body reverse bias (V_{DB} and V_{SB}) of 1.8 V. The retune loss of switches is less than -12 dB between 5 and 6 GHz.

The power measurement results of the switches at 5.825 GHz are shown in Fig. 4. When $V_{CTRL} = 3.6$ V and $V_{\overline{CTRL}} = 1.3$V, TX and ANT nodes are connected. P_{1dB} is 18 dBm for HSRSW and 17 dBm for LSRSW. This is an excellent result considering the voltage limitations of the 0.18-μm CMOS process. Output third intercept point (IP_3) was measured using a two-tone test. IP_3s for both switches are around 33 dBm.

The reliability test is also performed on switches. With ANT node open, which represents infinite VSWR, the switches were stressed for 1 h at input power 17 dBm for LSRSW and 18 dBm for HSRSW, respectively. No degradation was observed on insertion loss and isolation after the stress.

Besides the higher insertion loss for HSRSW, another difficulty for HSRSW is when the switch is integrated with other circuits, for example, LNA or PA, the substrate contacts of LNA and PA will reduce HSRSW substrate resistances, degrading switch performance, while this will slightly improve the performance of LSRSW. Because of these, low substrate resistance layouts are preferred for T/R switches in the 0.18-μm CMOS process. Lastly, the switches have similar insertion loss, isolationa and return loss as GaAs switches, though GaAs switches have higher P_{1dB} compression points [9], [10].

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